Remarks

Reconsideration of this application is requested. Claims 1-3, 6-7, 15, 18, and 21-22 have been amended. Claims 4-5, 9-10, 12, 16-17 and 19-20 have been canceled. Claims 1-3, 6-8, 11, 13-15, 18 and 21-22 remain in the application.

Specification

The Office action states that the amendment filed 2/27/2004 was objected to under 35 U.S.C. 132 because it introduced new matter into the disclosure. The Applicants disagree with the Examiner that new matter was added, noting that the figures show MOSFET devices for the charge protection device and it is well understood to one skilled in the art that source and drain regions form junction diodes. However, to further prosecution, that language has been removed from the claims.

Response to the 35 U.S.C. §112 Rejection, Claim 12

The Office Action states that claim 12 was objected to for a typographical error. By this amendment, claim 12 has been canceled.

Response to the 35 U.S.C. §112 Rejection, Claims 1 and 3

The Office Action states that claims 1 and 3 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. In particular, the Examiner concludes that "junction diodes formed by source and drain regions in a bulk region" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. As previously stated, the language referring to junction diodes has been removed from claims 1 and 3. These changes to these claims are believed to overcome the rejection based on 35 U.S.C. 112, first paragraph.

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Response to the 35 U.S.C. §112 Rejection, Claims 3 and 4

The Office Action states that claims 3 and 4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Applicants have amended claim 3 and canceled claim 4, and therefore, it is believed that Applicants' claim 3 complies with 35 U.S.C. 112, first paragraph, and the rejection should be removed.

Response to the 35 U.S.C. §102(b) Rejection

The Office Action rejects claims 1-3 under 35 U.S.C. 102(b) as being anticipated by Manning (US 6,163,044).

Rejection of claims 1-3

Applicants' claim 1 recites supplying a bulk region of the charge protection device with a first voltage potential through a first device when the integrated circuit is in operation, and supplying the bulk region with a second voltage potential through a second device when the integrated circuit experiences an electro-static discharge (ESD) event.

Manning does teach a FET device in FIG. 1 that has source and drain regions. A back-bias voltage is supplied that has a magnitude and a polarity which reverse biases the source-substrate junction, represented by diode 36 (see column 3, lines 3-6). However, the amended language of Applicants' claim 1 recites an integrated circuit with a charge protection device used during an electro-static discharge (ESD) which is not taught by Manning. Further, Applicants' claim 1 recites that the bulk region of the charge protection device receives a first voltage potential through a first device and a second voltage potential through a second device. Since Manning does not disclose a charge protection device, nor a bulk region that receives two different voltage potentials supplied by two different devices, this reference cannot anticipate Applicants' claim 1.

Rejected claims 2 and 3 depend directly from base claim 1 and are believed allowable for at least the same reasons as Applicants' claim 1.

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Response to the 35 U.S.C. §103(a) Rejection

The Office Action rejects claims 4-12, 15, 17-19 and 21 under 35 U.S.C. 103(a) as being unpatentable over Manning (US 6,163,044), in view of Maloney et al. and in view of Hirayama et al.

Rejection of claims 4-12

Note that Applicants' claims 4-5, 9-10, 12, 16-17 and 19-20 have been canceled by this amendment. Therefore, the rejection of claims 4-5 is now moot.

Manning teaches a FET device, where a back-bias voltage has a magnitude and a polarity to reverse bias the source-substrate junction.

Maloney et al. teach a long-channel resistive PFET to charge a capacitor, with an RC timer setting a time to shut off conduction of an ESD protection device.

Hirayama et al. teach detecting a normal operation mode and a standby mode of an IC. The bias potential from the substrate region to the source region of the transistor is altered to change the threshold voltage of the transistor based on a detected mode of operation. Hirayama et al. teach reducing power consumption by raising the threshold voltage of transistors during a standby mode.

Applicants' claim 6 recites a resistive element to supply a reverse bias to a bulk region and another device to supply a voltage potential that compensates the reverse bias to the bulk region.

Note that Manning, Maloney et al. and Hirayama et al. do not teach, either singularly or in combination, a resistive element to supply a reverse bias to a bulk region of a charge protection device and another device to supply the bulk region with a voltage potential that compensates the reverse bias (Applicants' claim 6). Since the relied upon reference do not teach or suggest this feature of Applicants' claim 6, the dependent claims 7, 8 and 11 are believed to be allowable over the relied upon references for at least the same reasons as claim 6.

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Rejection of claims 15 and 17

Applicants' amended claim 15 recites, among other things, a charge protection device coupled to an integrated circuit, the charge protection device comprising a first transistor and a second transistor arranged in series. A buffer has an output coupled to a gate terminal of the first transistor. A resistive element has a control terminal coupled to the output of the buffer and provides a signal to a gate terminal of the second transistor. A voltage divider includes serially connected transistors to supply a voltage potential to an input of the buffer.

Maloney in FIG. 8 teaches a charge protection device comprising a first transistor and a second transistor arranged in series (828 and 830). Maloney teaches a buffer (812 and 820) and a resistive element (812). But Maloney at least does not teach a resistive element having a control terminal coupled to the output of the buffer. Also, the Examiner states that Applicants' claim 17 was objected to as being dependent upon a rejected base claim, but allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The elements and limitations of claim 17 have been incorporated into base claim 15 and believed patentable over the relied upon prior art of Manning, Maloney et al. and Hirayama et al.

Rejection of claims 18-19 and 21

Applicants' amended claim 18 recites, among other things, a first transistor coupled between a positive power conductor and a ground power conductor to provide charge protection for an integrated circuit. A resistive element is coupled to provide a bulk region of the first transistor with a voltage potential that is greater than a voltage potential supplied on the positive power conductor. A second transistor couples the voltage potential supplied on the positive power conductor to the bulk region of the first transistor when the integrated circuit experiences an electro-static discharge (ESD) event.

Claim 18 recites that the bulk region of the transistor that provide charge protection for an integrated circuit receives a voltage potential through a resistive element and a voltage potential supplied on the positive power

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conductor through a second transistor to the bulk region. At least this feature of Applicants' claim 18 is not found in either Manning, Maloney et al. or Hirayama et al. Therefore, the combination of these prior art references cannot provide a valid U.S.C. 103(a) rejection.

The dependent claim 19 has been canceled by this amendment. Claim 21 depends directly from claim 18 and is believed to be allowable over the relied upon references for at least the same reasons as claim 18.

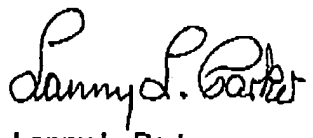
Conclusion

The foregoing is submitted as a full and complete response to the Office Action mailed September 10, 2004, and it is submitted that claims 1-3, 6-8, 11, 13-15, 18 and 21-22 are in condition for allowance. Reconsideration of the rejection of claims is requested and the allowance of amended claims is earnestly solicited.

Should it be determined that a fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #50-0221.

If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (480) 715-5388 is respectfully solicited.

Respectfully submitted,
Lawrence T. Clark



Lanny L. Parker
Patent Agent
Reg. No. 44,281

c/o Blakely, Sokoloff, Taylor & Zafman, LLP
12400 Wilshire Blvd., Seventh Floor
Los Angeles, CA 90025-1026
(503) 264-0967

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